SMALL-OUTLINE DDR SDRAM MODULE

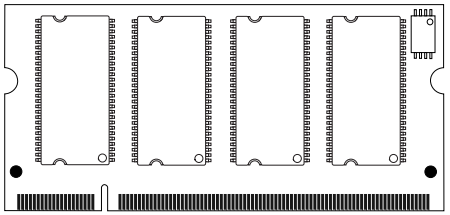
MT16VDDS6464H - 512MB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/moduleds

FEATURES

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- Fast data transfer rates PC1600 or PC2100
- Utilizes 200 MT/s and 266 MT/s DDR (Twin-Die) SDRAM components
- 512MB (64 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +2.5V ±0.2V
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK# (can be multiple clock, i.e., pairs CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold-plated edge contacts

200-Pin SODIMM (Twin-Die)
MO-224



OPTIONS — MARKING

• Package	
200-pin SODIMM (gold)	G
• Frequency/CAS Latency	
133 MHz (266 MT/s) CL = 2	-26A
133 MHz (266 MT/s) CL = 2.5	-265
100 MHz (200 MT/s) CL = 2	-202

ADDRESS TABLE

	512MB
Refresh Count	8K
Row Addressing	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)
Device Configuration	32 Meg x 8
Column Addressing	1K (A0–A9)
Module Bank Addressing	2 (S0#, S1#)

PART NUMBERS AND TIMING PARAMETERS

PART NUMBER	PART MARKING	MODULE DENSITY	CONFIGURATION	TRANSFER RATE	MEMORY CLOCK/ DATA BIT RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT16VDDS6464HG-26A__	-26A	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT16VDDS6464HG-265__	-265	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT16VDDS6464HG-202__	-202	512MB	64 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16VDDS6464HG-265A1

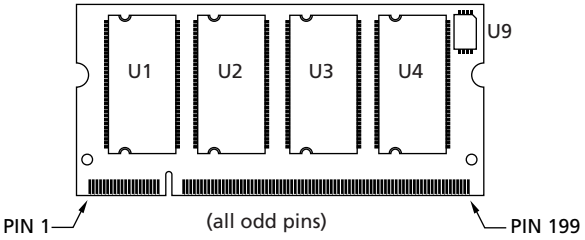
PIN ASSIGNMENT (200-Pin SODIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
5	DQ0	55	DQ24	105	A7	155	V_{DD}
7	DQ1	57	V_{DD}	107	A5	157	V_{DD}
9	V_{DD}	59	DQ25	109	A3	159	V_{SS}
11	DQS0	61	DQS3	111	A1	161	V_{SS}
13	DQ2	63	V_{SS}	113	V_{DD}	163	DQ48
15	V_{SS}	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	V_{DD}
19	DQ8	69	V_{DD}	119	WE#	169	DQS6
21	V_{DD}	71	DNU	121	S0#	171	DQ50
23	DQ9	73	DNU	123	NC	173	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
27	V_{SS}	77	DNU	127	DQ32	177	DQ56
29	DQ10	79	DNU	129	DQ33	179	V_{DD}
31	DQ11	81	V_{DD}	131	V_{DD}	181	DQ57
33	V_{DD}	83	DNU	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
39	V_{SS}	89	DNU	139	DQ35	189	DQ59
41	DQ16	91	DNU	141	DQ40	191	V_{DD}
43	DQ17	93	V_{DD}	143	V_{DD}	193	SDA
45	V_{DD}	95	CKE1	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	V_{DDSPD}
49	DQ18	99	A12	149	V_{SS}	199	NC

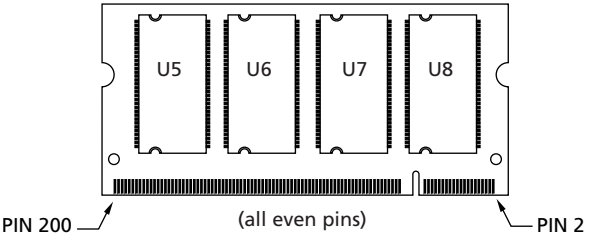
PIN ASSIGNMENT (200-Pin SODIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
6	DQ4	56	DQ28	106	A6	156	V_{DD}
8	DQ5	58	V_{DD}	108	A4	158	CK1#
10	V_{DD}	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	V_{SS}
14	DQ6	64	V_{SS}	114	V_{DD}	164	DQ52
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	V_{DD}
20	DQ12	70	V_{DD}	120	CAS#	170	DM6
22	V_{DD}	72	DNU	122	S1#	172	DQ54
24	DQ13	74	DNU	124	NC	174	V_{SS}
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
28	V_{SS}	78	DNU	128	DQ36	178	DQ60
30	DQ14	80	DNU	130	DQ37	180	V_{DD}
32	DQ15	82	V_{DD}	132	V_{DD}	182	DQ61
34	V_{DD}	84	DNU	134	DM4	184	DM7
36	V_{DD}	86	DNU	136	DQ38	186	V_{SS}
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
42	DQ20	92	V_{DD}	142	DQ44	192	V_{DD}
44	DQ21	94	V_{DD}	144	V_{DD}	194	SA0
46	V_{DD}	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	V_{SS}	200	NC

Front View (Twin-Die)



Back View



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
118, 119, 120	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#) define the command being entered.
35, 37, 158, 160	CK0, CK0# CK1, CK1#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK0#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
95, 96	CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE0 LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE0 is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
121, 122	S0#, S1#	Input	Chip Selects: S0# or S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# or S1# is registered HIGH. S0# or S1# is considered part of the command code.
116, 117	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
99, 100, 101, 102, 105, 106, 107, 108, 109, 110, 111, 112, 115	A0-A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
1, 2	V_{REF}	Input	SSTL_2 reference voltage.
195	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.

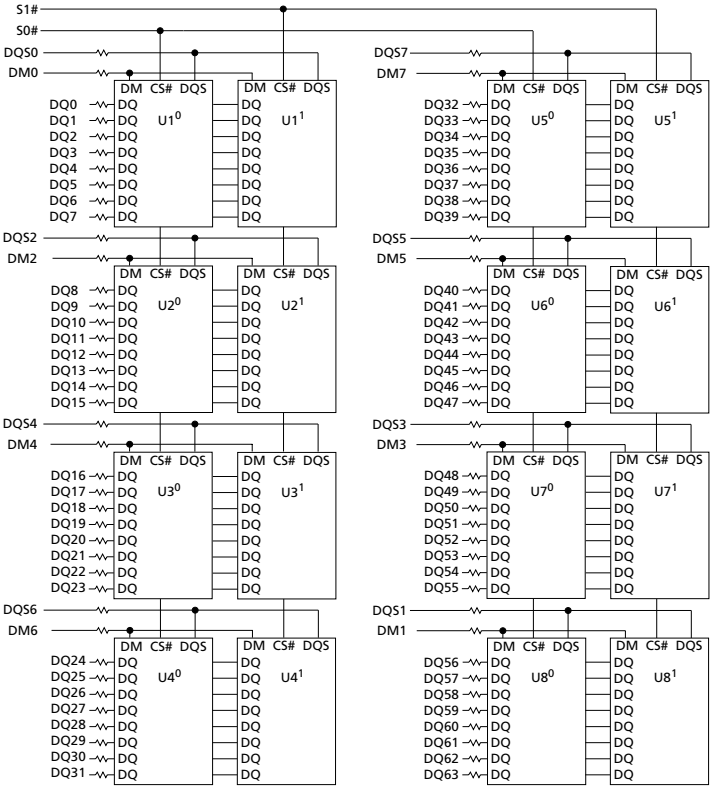
NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

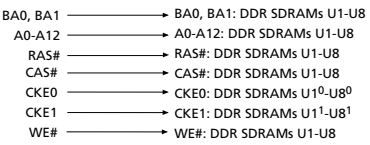
PIN DESCRIPTIONS (continued)

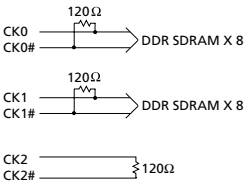
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
194, 196, 198	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
193	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
12, 26, 48, 62, 134, 148, 170, 184	DM0-DM7	Input	Data Write Mask. DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
11, 25, 47, 61, 133, 147, 169, 183	DQS0-DQS7	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
5, 6, 7, 8, 13, 14, 17, 18, 19, 20, 23, 24, 29, 30, 32, 41, 42, 43, 44, 49, 50, 53, 54, 55, 56, 59, 60, 65, 66, 67, 68, 127, 128, 129, 130, 135, 136, 139, 140, 141, 142, 145, 146, 151, 152, 153, 154, 163, 164, 165, 166, 171, 172, 175, 176, 177, 178, 181, 182, 187, 188, 189, 190	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
9, 10, 21, 22, 33, 34, 36, 45, 46, 57, 58, 69, 70, 81, 82, 92, 93, 94, 113, 114, 131, 132, 143, 144, 155, 156, 157, 167, 168, 179, 180, 191, 192	V_{DD}	Supply	Power Supply: +2.5V ±0.2V.
3, 4, 15, 16, 27, 28, 38, 39, 40, 51, 52, 63, 64, 75, 76, 87, 88, 90, 103, 104, 125, 126, 137, 138, 149, 150, 159, 161, 162, 173, 174, 185, 186	V_{SS}	Supply	Ground.
197	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
85, 97, 98, 123, 124, 199, 200	NC	—	No Connect: These pins should be left unconnected.
71, 72, 73, 74, 77, 78, 79, 80, 83, 84, 86, 89, 91	DNU	—	Do Not Use: These pins are not connected on this module, but are assigned pins on other modules in this product family.

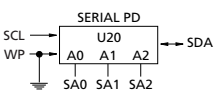
NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

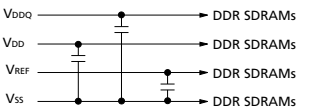
FUNCTIONAL BLOCK DIAGRAM
512MB Module











U1 - U8: MT46V32M8S2TG DDR SDRAM twin-die

NOTE: 1. All resistor values are 22 ohms unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

GENERAL DESCRIPTION

The MT16VDDS6464H is a high-speed CMOS, dynamic random-access, 512MB memory module organized in a x64 configuration. This module uses internally configured quad-bank DDR SDRAM devices.

This DDR SDRAM module uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

This DDR SDRAM module operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM module is burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0-A12 select device row. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

This DDR SDRAM module provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAM modules, the pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 256Mb DDR SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This DDR SDRAM module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

REGISTER DEFINITION

MODE REGISTER

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in the Mode Register Diagram. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A12 when the burst length is set to two, by A2-A12

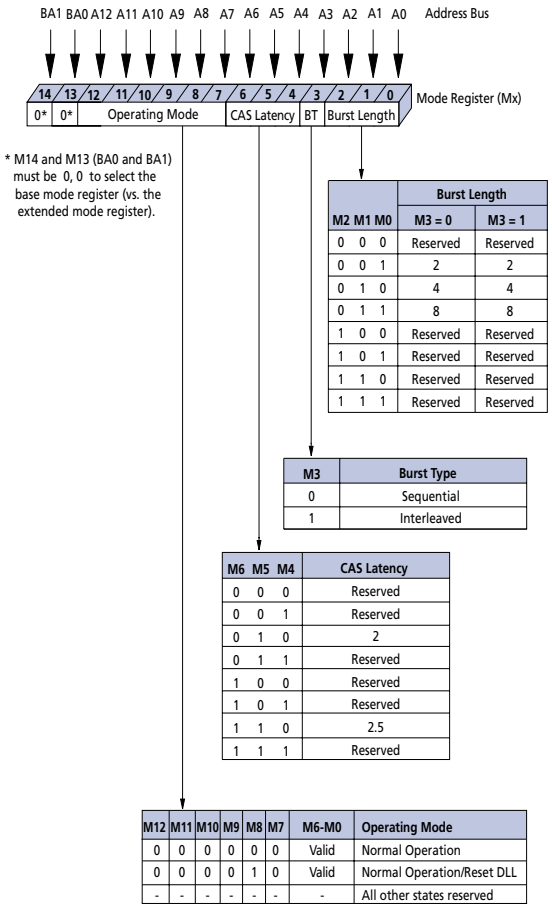
when the burst length is set to four and by A3-A12 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table.

Mode Register Definition Diagram



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:
1. For a burst length of two, A1-A12 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A12 select the four-data-element block; A0-A1 select the first access within the block.
3. For a burst length of eight, A3-A12 select the eight-data-element block; A0-A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

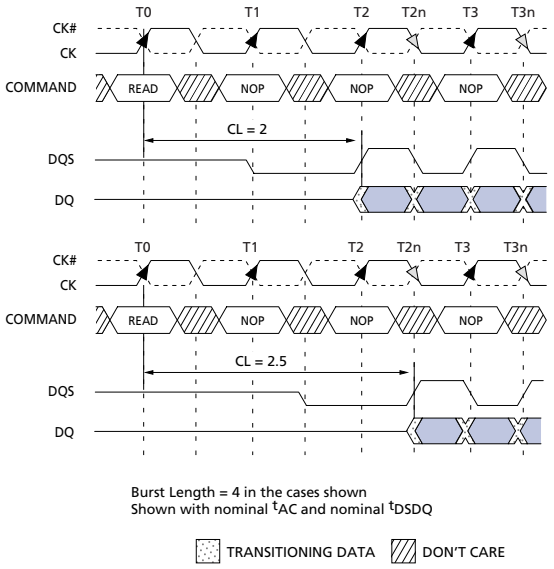
Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in CAS Latency Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency Diagram



CAS Latency (CL) Table

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CL = 2	CL = 2.5
-26A	75 ≤ f ≤ 133	75 ≤ f ≤133
-265	75 ≤ f ≤ 100	75 ≤ f ≤133
-202	75 ≤ f ≤ 100	75 ≤ f ≤125

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A12 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in the Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

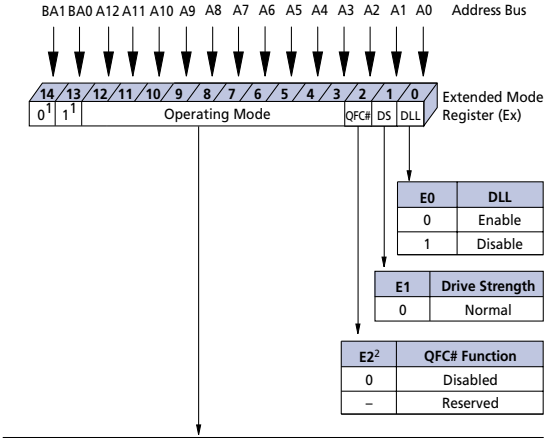
Output Drive Strength

The normal full drive strength for all outputs are specified to be SSTL2, Class II. For detailed information on output drive strength operation, refer to 256Mb DDR SDRAM component data sheet.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Extended Mode Register Definition Diagram



E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2, E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE: 1. E14 and E13 (BA0 and BA1) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

COMMANDS

The Truth Tables below provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 256Mb DDR SDRAM component data sheet.

TRUTH TABLE – COMMANDS

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

TRUTH TABLE – DM OPERATION

(Note: 10)

NAME (FUNCTION)	DM	DQs
WRITE Enable	L	Valid
WRITE Inhibit	H	X

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A12 provide the op-code to be written to the selected mode register.
3. BA0-BA1 provide device bank address and A0-A12 provide device row address.
4. BA0-BA1 provide device bank address; A0-A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls device row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data; provided coincident with the corresponding data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} ..... -1V to +3.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} ..... -1V to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS} ..... -1V to +3.6V
Voltage on I/O Pins
Relative to V_{SS} ..... -0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1–5, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	2.3	2.7	V	32, 36
I/O Supply Voltage		$V_{DD}Q$	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		V_{REF}	0.49 × $V_{DD}Q$	0.51 × $V_{DD}Q$	V	6, 39
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 39
Input High (Logic 1) Voltage		V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	25
Input Low (Logic 0) Voltage		V_{IL}(DC)	-0.3	V_{REF} - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command address	I_I	-32	32	µA	48
	CK, CK#		-16	16		
	DQ, DQS, DQM		4	4		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-10	10	µA	48
OUTPUT LEVELS: High Current (V_{OUT} = $V_{DD}Q$-0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA	33, 34
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

AC INPUT OPERATING CONDITIONS

(Notes: 1–5, 12, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	V_{IL}(AC)	–	V_{REF} - 0.310	V	12, 25, 35
I/O Reference Voltage	V_{REF}(AC)	0.49 × $V_{DD}Q$	0.51 × $V_{DD}Q$	V	6

IDD SPECIFICATIONS AND CONDITIONS*

(Notes: 1-5, 8, 10, 12; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V)

			MAX			
PARAMETER/CONDITION		**SYMBOL**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	TBD	TBD	mA	20, 43
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	TBD	TBD	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)		IDD2P	24	24	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2N	280	240	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	TBD	TBD	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	280	240	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	TBD	TBD	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	TBD	TBD	mA	20
AUTO REFRESH CURRENT	tRC = tRC(MIN)	IDD5	TBD	TBD	mA	20, 45
	tRC = 7.8125µs	IDD5A	48	48	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	TBD	TBD	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, tRC = tRC (MIN); tCK = tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		IDD7	TBD	TBD	mA	20, 44

*DDR SDRAM components only.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1–5, 12–15, 29; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

AC CHARACTERISTICS			-26A		-265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		^tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
Clock cycle time	CL = 2.5	^tCK (2.5)	7.5	13	7.5	13	8	13	ns	40,47
	CL = 2	^tCK (2)	7.5	13	10	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS		^tDH	0.5		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS		^tDS	0.5		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#		^tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.5		0.5		0.6	ns	22, 23
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		0.2		^tCK	
Half clock period		^tHP	^tCH, ^tCL		^tCH, ^tCL		^tCH, ^tCL		ns	30
Data-out high-impedance window from CK/CK#		^tHZ		+0.75		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#		^tLZ	-0.75		-0.75		-0.8		ns	16, 38
Address and control input hold time (fast slew rate)		^tIH_F	.90		.90		1.1		ns	12
Address and control input setup time (fast slew rate)		^tIS_F	.90		.90		1.1		ns	12
Address and control input hold time (slow slew rate)		^tIH_S	1		1		1.1		ns	12
Address and control input setup time (slow slew rate)		^tIS_S	1		1		1.1		ns	12
LOAD MODE REGISTER command cycle time		^tMRD	15		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS		^tHP -^tQHS		^tHP-^tQHS		ns	22, 23
Data hold skew factor		^tQHS		0.75		0.75		1	ns	
ACTIVE to PRECHARGE command		^tRAS	40	120,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command		^tRAP	20		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	65		65		70		ns	
AUTO REFRESH command period		^tRFC	75		75		80		ns	45
ACTIVE to READ or WRITE delay		^tRCD	20		20		20		ns	
PRECHARGE command period		^tRP	20		20		20		ns	
DQS read preamble		^tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	^tCK	37
DQS read postamble		^tRPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	15		15		15		ns	
DQS write preamble		^tWPRE	0.25		0.25		0.25		^tCK	
DQS write preamble setup time		^tWPRES	0		0		0		ns	18, 19
DQS write postamble		^tWPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	17
Write recovery time		^tWR	15		15		15		ns	
Internal WRITE to READ command delay		^tWTR	1		1		1		^tCK	
Data valid output window		na	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	22
REFRESH to REFRESH command interval		^tREFC		70.3		70.3		70.3	µs	21
Average periodic refresh interval		^tREFI		7.8		7.8		7.8	µs	21
Terminating voltage delay to V_{DD}		^tVTD	0		0		0		ns	
Exit SELF REFRESH to non-READ command		^tXSNR	75		75		80		ns	
Exit SELF REFRESH to READ command		^tXSRD	200		200		200		^tCK	

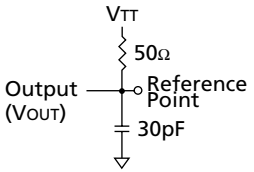
CAPACITANCE (All Modules)

(Note: 11; notes appear following parameter tables)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQs, DQSs	C_{IO}	TBD	TBD	pF
Input Capacitance: Command and Address, S0#	C_{I1}	TBD	TBD	pF
Input Capacitance: CK0, CK0#, CK1, CK1#	C_{I2}	TBD	TBD	pF
Input Capacitance: CKE0, CKE1	C_{I3}	TBD	TBD	pF

NOTES

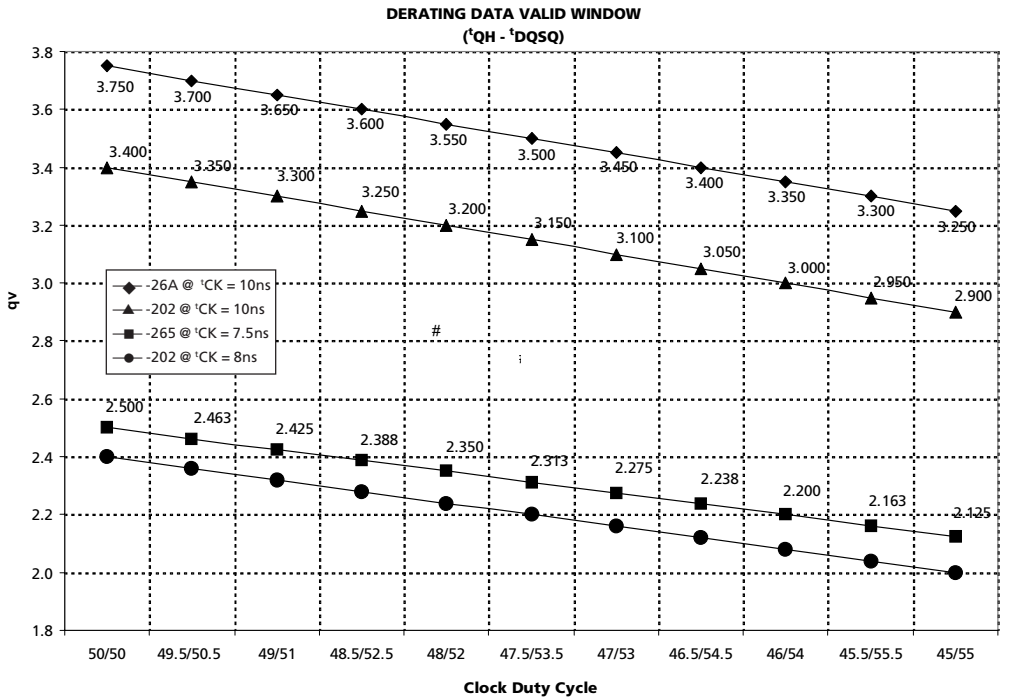
1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -26A and -202, CL = 2.5 for -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, $V_{OUT(DC)}$ = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -75 with slew rates 1V/ns and faster, ^tIS and ^tIH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: ^tIS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. ^tIH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^tHZ and ^tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^tDQSS.
20. MIN (^tRC or ^tRFC) for I_{DD} measurements is the smallest multiple of ^tCK that meets the minimum absolute value for the respective parameter. ^tRAS (MAX) for I_{DD} measurements is the largest multiple of ^tCK that meets the maximum absolute value for ^tRAS.

NOTES (continued)

21. The refresh period 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
23. Referenced to each output group: x8 = DQS with DQ0-DQ7.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.



NOTES (continued)

28. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until $^{t}RAS_{(MIN)}$ can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than $^{1}/_{3}$ of the clock and not more than +400mV or 2.9 volts, whichever is less. Any negative glitch must be less than $^{1}/_{3}$ of the clock cycle and not exceed either -300mV or 2.2 volts, whichever is more positive.
33. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0 Volt.
34. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. V_{IH} overshoot: $V_{IH}(MAX) = V_{DD}Q+1.5V$ for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL}(MIN) = -1.5V$ for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. V_{DD} and $V_{DD}Q$ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^{t}HZ (MAX) and the last DVW. ^{t}HZ (MAX) will prevail over $^{t}DQSCK$ (MAX) + $^{t}RPST$ (MAX) condition. ^{t}LZ (MIN) will prevail over $^{t}DQSCK$ (MIN) + $^{t}RPRE$ (MAX) condition.

Figure A
Pull-Down Characteristics

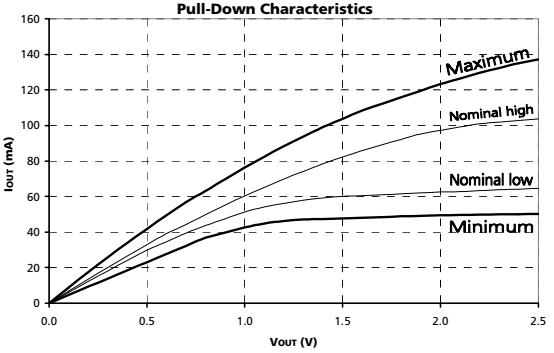
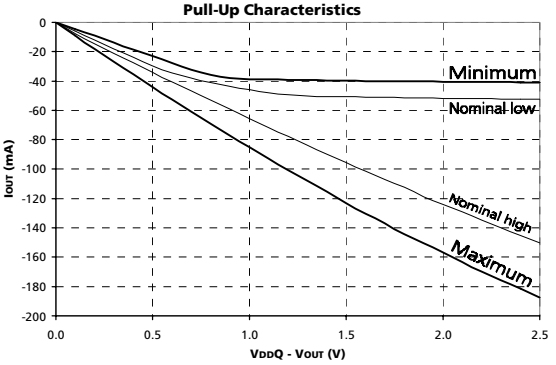


Figure B
Pull-Up Characteristics



NOTES (continued)

38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, V_{DDQ}, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{DD}/V_{DDQ} are 0 volts, provided a minimum of 42 ohms of series resistance is used between the V_{TT} supply and the input pin.
40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. $^{t}RAP \geq {}^{t}RCD$.
42. For the -265 and -26A, $I_{DD}3N$ is specified to be 35mA at 100 MHz.
43. Random addressing changing 50% of data changing at every transfer.
44. Random addressing changing 100% of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 1
Data Validity

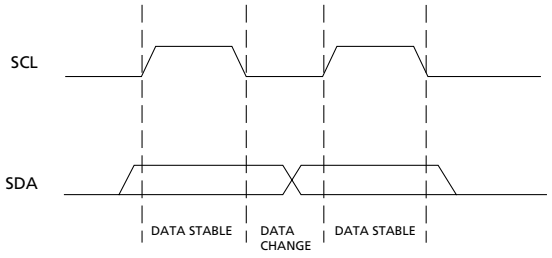


Figure 2
Definition of Start and Stop

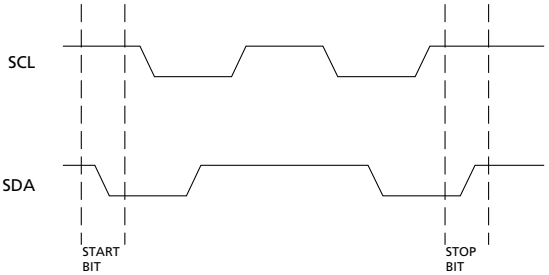
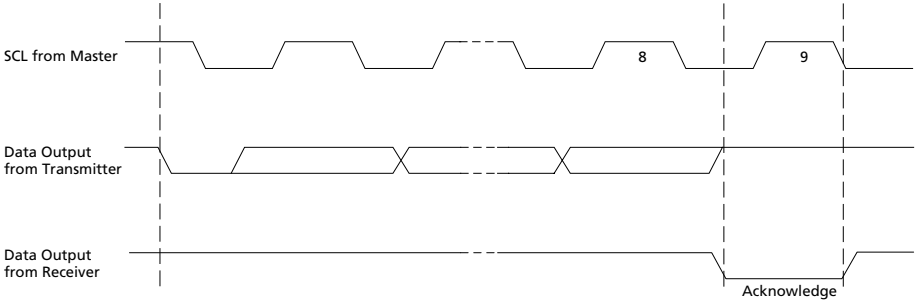


Figure 3
Acknowledge Response From Receiver



EEPROM DEVICE SELECT CODE

Note: The most significant bit (b7) is sent first.

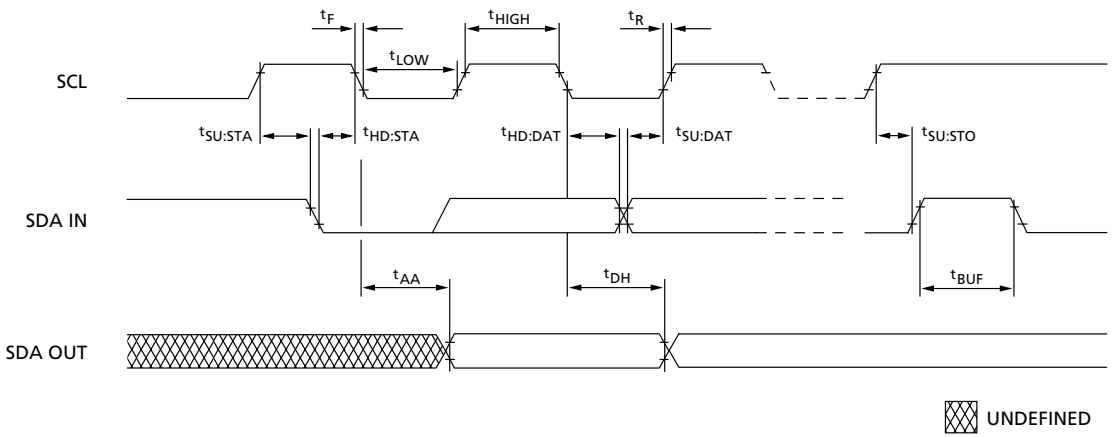
	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	RW
Protection Register Select Code	0	1	1	0	E2	E1	E0	RW

EEPROM OPERATING MODES

MODE	RW BIT	WC[1]	BYTES	INITIAL SEQUENCE
Current Address Read	1	X	1	START, Device Select, RW = '1'
Random Address Read	0	X	1	START, Device Select, RW = '0', Address
	1	X	1	reSTART, Device Select, RW = '1'
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, RW = '0'
Page Write	0	V_{IL}	≤ 16	START, Device Select, RW = '0'

NOTE: 1. X = V_{IH} or V_{IL}.

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DDSPD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Notes: 1) (V_{DDSPD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	2

NOTE: 1. All voltages referenced to V_{SS}.
2. The refresh period is 64ms. This equates to an average refresh rate of 15.625µs. However, an AUTO REFRESH command must be asserted at least once every 31.2µs; burst refreshing or postings greater than 2 are not allowed.

SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT16VDDS6464H
0	NUMBER OF SPD BYTES USED BY MICRON	128	80
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	256	08
2	FUNDAMENTAL MEMORY TYPE	SDRAM DDR	07
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	13	0D
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	10	0A
5	NUMBER OF PHYSICAL BANKS ON DIMM	2	02
6	MODULE DATA WIDTH	64	40
7	MODULE DATA WIDTH (continued)	0	00
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	SSTL 2.5V	04
9	SDRAM CYCLE TIME, (^{t}CK) (CAS LATENCY = 2.5) (Note 2)	7 (-26A) 7.5 (-265) 8 (-202)	70 75 80
10	SDRAM ACCESS FROM CLOCK,(^{t}AC) (CAS LATENCY = 2.5)	0.75 (-26A/-265) 0.8 (-202)	75 80
11	MODULE CONFIGURATION TYPE	Non-ECC	00
12	REFRESH RATE/TYPE	7.8µs/SELF	82
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	x8	08
14	ERROR-CHECKING SDRAM DATA WIDTH	Non-ECC	00
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	1 clock	01
16	BURST LENGTHS SUPPORTED	2, 4, 8	0E
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04
18	CAS LATENCIES SUPPORTED	2.5	0C
19	CS LATENCY	0	01
20	WE LATENCY	1	02
21	SDRAM MODULE ATTRIBUTES	Unbuffered/Diff. Clock	20
22	SDRAM DEVICE ATTRIBUTES: GENERAL	Fast/concurrent AP	C0
23	SDRAM CYCLE TIME, (^{t}CK) (CAS latency = 2) (Note 2) (CAS LATENCY = 2)	7.5 (-26A) 10 (-265/-202)	75 A0
24	SDRAM ACCESS FROM CK , (^{t}AC) (CAS latency = 2) (CAS LATENCY = 2)	7.5 (-26A/-265) 8 (-202)	75 80
25	SDRAM CYCLE TIME, (^{t}CK) (CAS LATENCY = 1.5)	N/A	00
26	SDRAM ACCESS FROM CK , (^{t}AC) (CAS LATENCY = 1.5)	N/A	00
27	MINIMUM ROW PRECHARGE TIME, (^{t}RP)	20 ns	50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (^{t}RRD)	15 ns	3C
29	MINIMUM RAS# TO CAS# DELAY, (^{t}RCD)	20 ns	50
30	MINIMUM RAS# PULSE WIDTH, (^{t}RAS) (Note 3)	45 (-26A/-265) 40 (-202)	2D 28
31	MODULE BANK DENSITY	256MB	40

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. Device latencies used for SPD values.
3. The value of ^{t}RAS used for -26A/-265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec value is 40 ns.

SERIAL PRESENCE-DETECT MATRIX (continued)

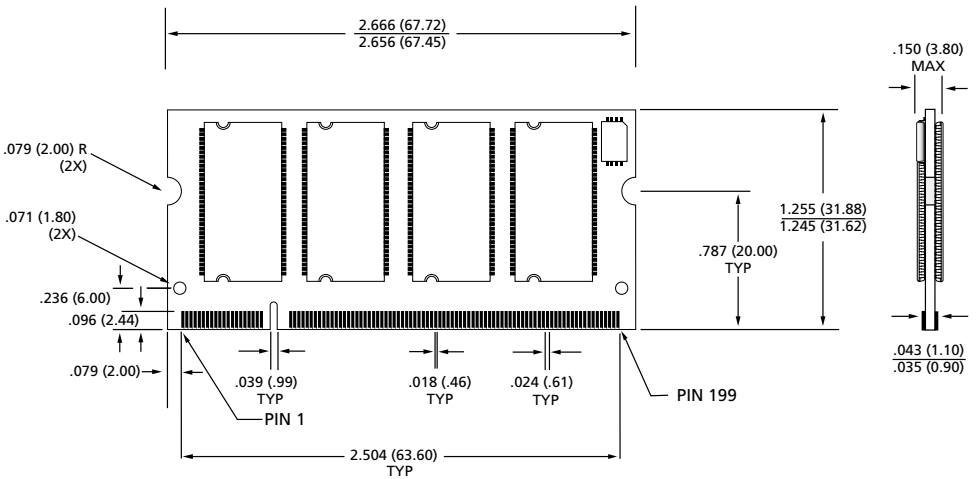
(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT16VDDS6464H
32	ADDRESS AND COMMAND SETUP TIME, (^{t}IS)	1.0 (-26A/-265) 1.1 (-202)	A0 B0
33	ADDRESS AND COMMAND HOLD TIME, (^{t}IH)	1.0 (-26A/-265) 1.1 (-202)	A0 B0
34	DATA/DATA MASK INPUT SETUP TIME, (^{t}DS)	0.5 (-26A/-265) 0.6 (-202)	50 60
35	DATA/DATA MASK INPUT HOLD TIME, (^{t}DH)	0.5 (-26A/-265) 0.6 (-202)	50 60
36-40	RESERVED		00
41	MIN ACTIVE AUTO REFRESH TIME (^{t}RC)	65ns (-26A/-265) 70ns (-202)	41 46
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (^{t}RFC)	75ns (-26A/-265) 80ns (-202)	4B 50
43	SDRAM DEVICE MAX CYCLE TIME (^{t}CK$_{MAX}$)	^{t}CK (MAX) = 13.0ns	34
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (^{t}DQSQ)	0.5ns (-26A/-265) 0.6ns (-202)	32 3C
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (^{t}QHS)	.75ns (-26A/-265) 1.0ns (-202)	75 A0
46-61	RESERVED		00
62	SPD REVISION	Initial Release 0.0	00
63	CHECKSUM FOR BYTES 0-62	-26A -265 -202	D7 07 A2
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C
65-71	MANUFACTURER'S JEDEC ID CODE (continued)		00
72	MANUFACTURING LOCATION	01–11	01–B0
73-90	MODULE PART NUMBER (ASCII)	x	
91	PCB IDENTIFICATION CODE	1-9	01-09
92	IDENTIFICATION CODE (continued)	0	00
93	YEAR OF MANUFACTURE IN BCD		x
94	WEEK OF MANUFACTURE IN BCD		x
95-98	MODULE SERIAL NUMBER		x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		–

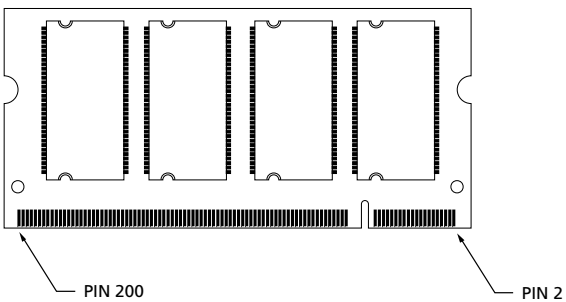
NOTE: 1. x = Variable Data.

200-PIN SODIMM (TWIN-DIE)
512MB Module

FRONT VIEW



BACK VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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